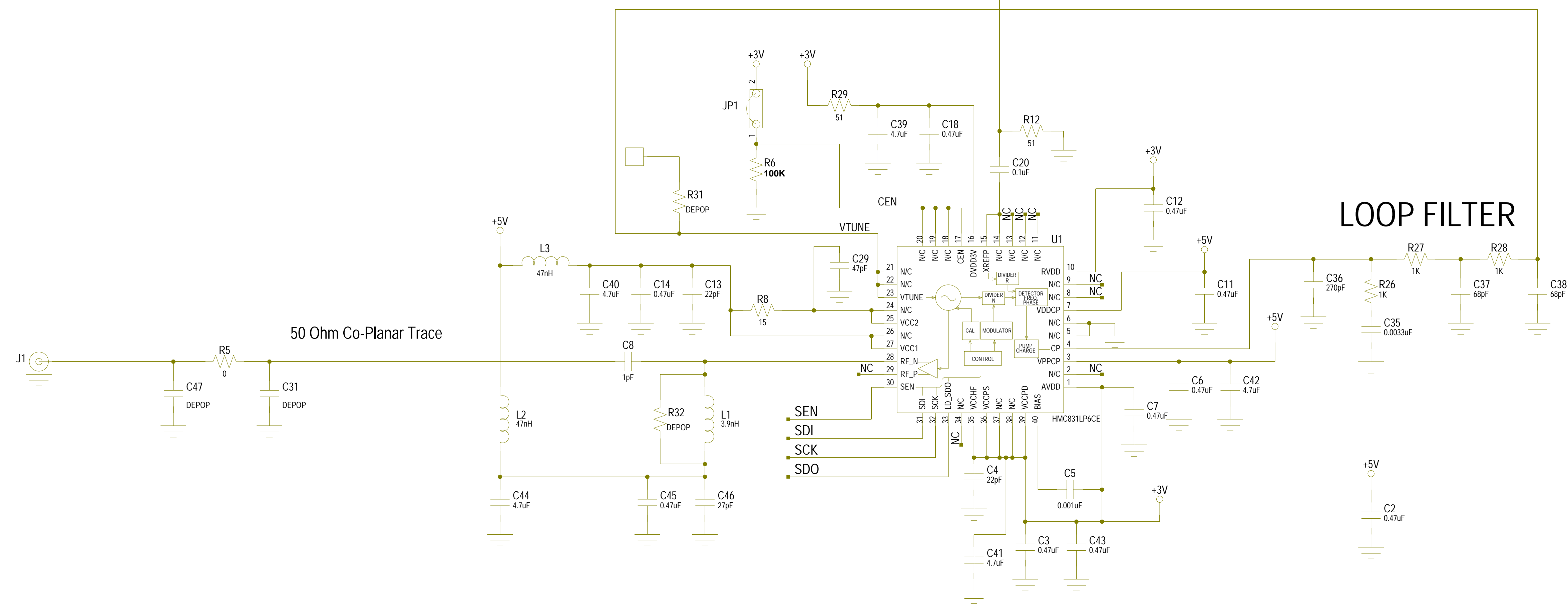
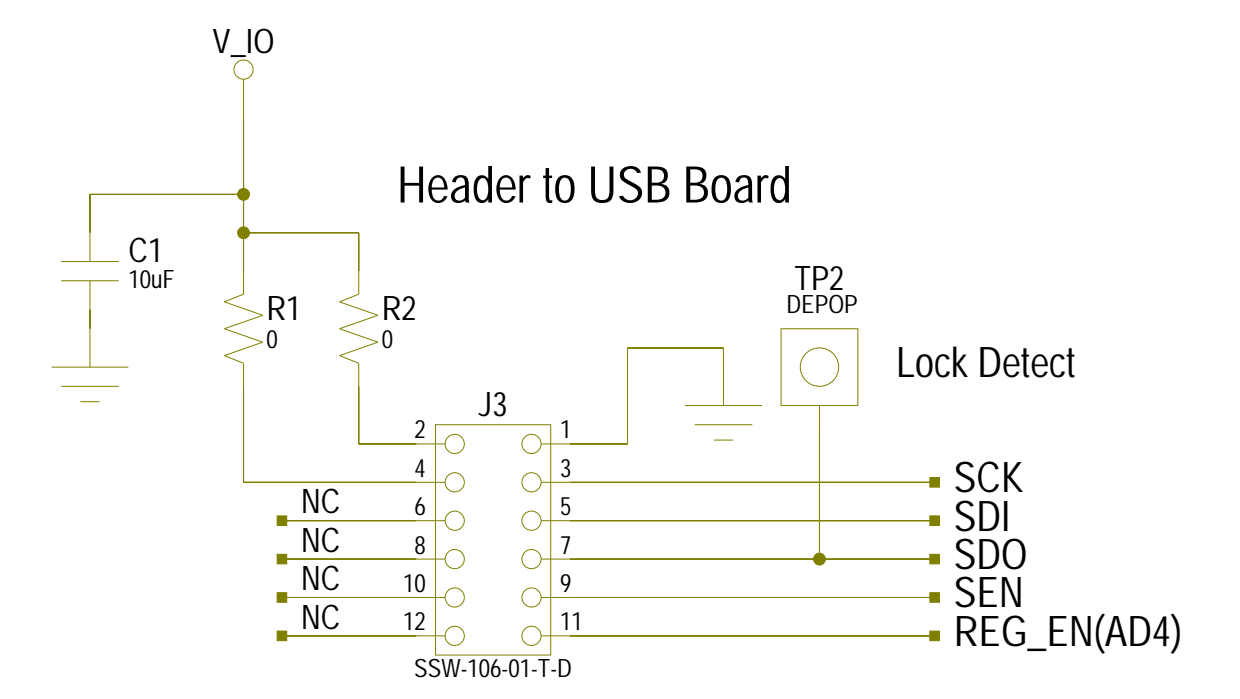
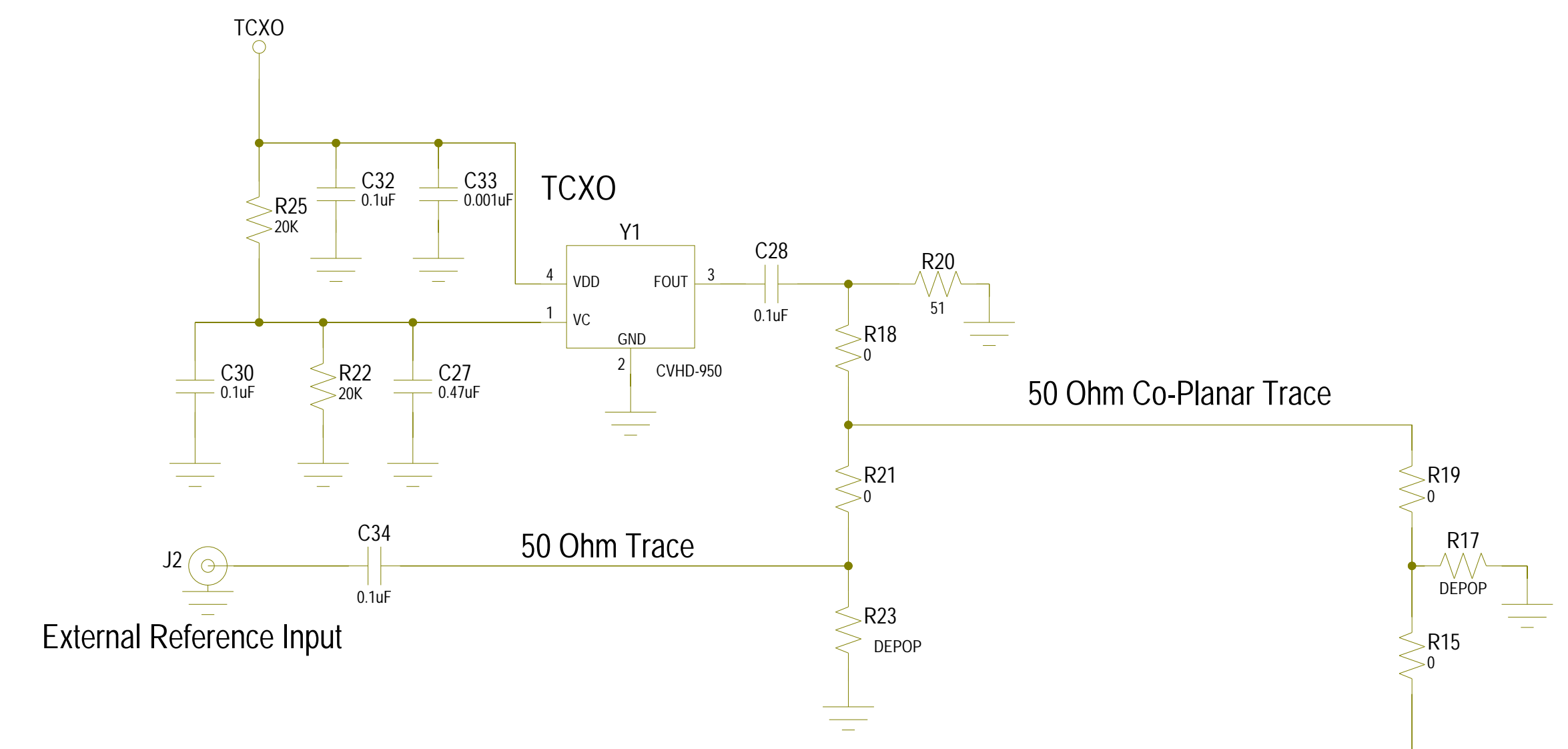
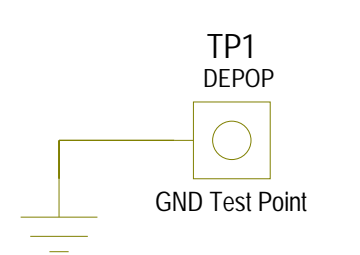


REVISIONS					
REV	ECN#	ZONE	DESCRIPTION	NAME	DATE
A	20100115	.....	PRODUCTION RELEASE PER ECN 20100115	D. YOUNG	24/01/10
B	CP121275	.....	PRODUCTION CHANGE PER CP 121275	V. VADUVA	09/14/2012

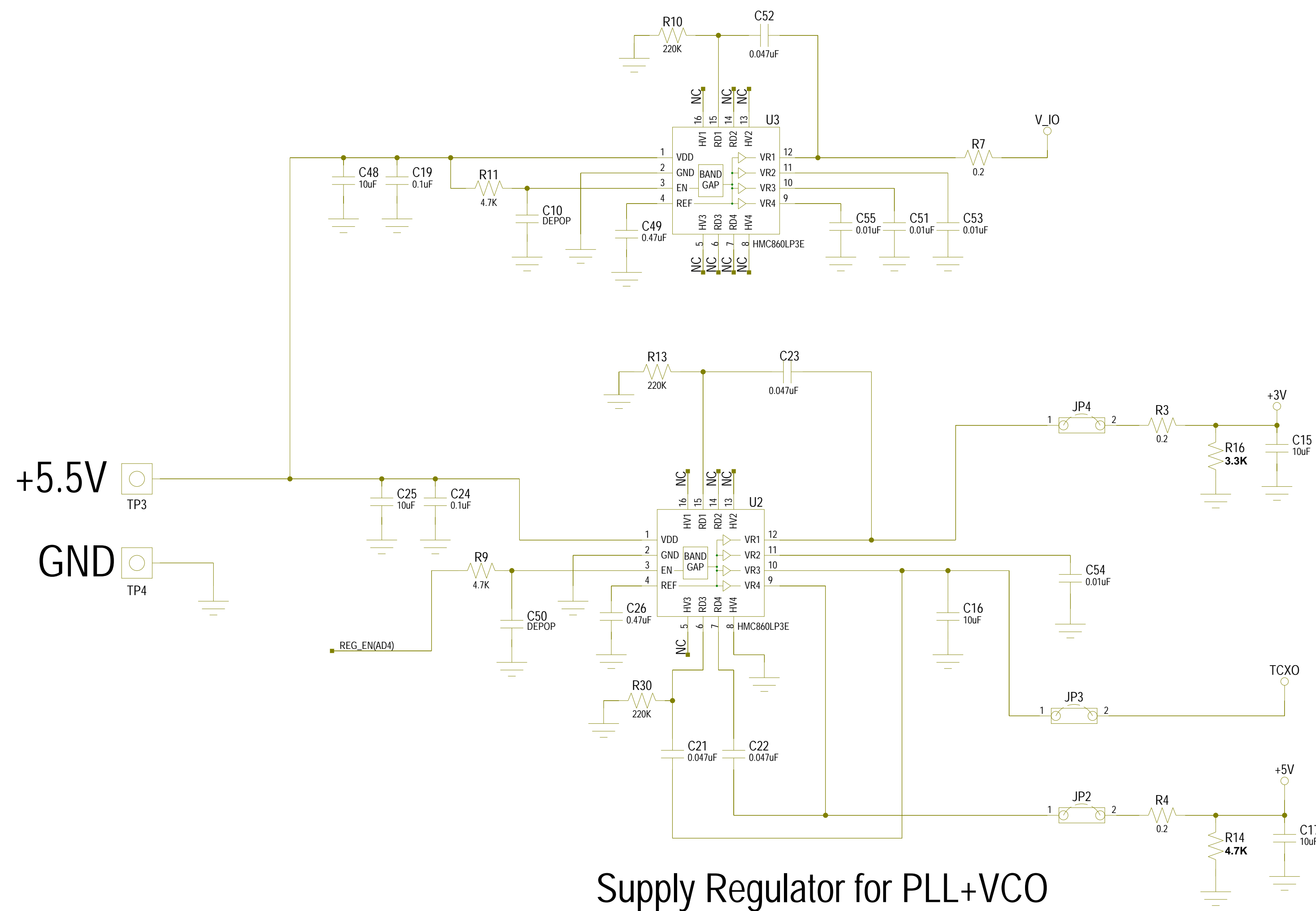


## HMC831LP6CE Integrated PLL & VCO Eval




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TITLE SCH, CUSTOMER EVALALUATION PLL & VCO			
PROJECT		SHEET 1 OF 2	
DRAWING #:	129271	CODE ID NO:	1CN88
DRAWN BY:	D.YOUNG	DATE:	10/01/2010
		SIZE:	D
		REV:	B



A recommended design practice is to connect the regulator Enable Pin #3 through a 4.7kOhm resistor to the system microcontroller/FPGA for power management control  
 Small series resistors required in VR1 and VR4 output paths, as shown

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<b>TITLE</b> SCH, CUSTOMER EVALALUTION PLL & VCO	
<b>PROJECT</b> DRAWING #: 129271	
<b>SHEET</b> 2 OF 2 <small>CODE ID NO. SIZE REV</small>	
DRAWN BY: D.YOUNG	DATE: 10/01/2010
1CN88 D B	